(9) CLAIMS

1. A semiconductor MOSFET structure having improved electrostatic discharge tolerance, the structure comprising:

a semiconductor substrate having an active device surface;

in said surface, a MOSFET source region and a MOSFET drain region separated by a channel region;

a P-type dopant region subjacent said drain region and having a dopant concentration and predetermined dimensions such inherent parasitic transistor gain of said MOSFET structure is increased.

2. The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set for increasing drain-to-substrate capacitance thereby.

3. The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set such that the MOSFET trigger voltage is decreased thereby.

4. The structure as set forth claim 1 wherein breakdown voltage of said parasitic transistor is tailored by depth of the P-type dopant region with respect to said surface

and said substrate.

5. The structure as set forth in claim 1 wherein said MOSFET is a N-channel MOSFET located in a P-type dopant well in said epitaxial layer and surface concentration of the dopant ions in the P-deep region is approximately an order of magnitude greater than that of the dopant ions at the P-well 209 surface concentration.

6. The structure as set forth in claim 3 comprising:

a pair of MOSFETs, including a N-MOSFET, and a P-MOSFET, wherein said N-MOSFET and said P-MOSFET are connected in a push-pull configuration.

7. The structure as set forth in claim 6 wherein the P-deep implant region in both the P-MOSFET and the N-MOSFET reduces effective base width of parasitic transistors therein via reduction of substrate-to-drain spacing.

8. An integrated circuit electrostatic discharge protection device for an IC Input-output pad, the device comprising:

a N-MOSFET;

a P-MOSFET, wherein said N-MOSFET and P-MOSFET are connected in a push-pull configuration with drain regions thereof connected to said Input-output pad; and

both said N-MOSFET and said P-MOSFET including a P-type dopant region substantially subjacent respective the drain regions of each such that P-MOSFET parasitic PNP transistor gain and N-MOSFET parasitic NPN transistor gain is increased

thereby.

9. An electrostatic discharge protection circuit for an IC having at least one I/O pad and at least one VCC pad having a electrically grounded electrostatic discharge protection device connected thereto, the circuit comprising:

a N-GCMOSFET having a first drain region connected to said I/O pad, a first gate region connected to electrical ground, and a first source region connected to electrical ground; and

a P-GCMOSFET having a second drain region connected to said I/O pad, a second gate region connected to said VCC pad, and a second source region connected to said VCC pad,

wherein said first drain region has a P-type dopant region substantially subjacent thereto for enhancing parasitic NPN transistor gain thereof, and said second drain region has a P-type dopant region substantially subjacent thereto for enhancing parasitic PNP transistor gain thereof.

10. The circuit as set forth in claim 9 wherein when the I/O pad experiences an electrostatic discharge event, the P-type drain, acting as the emitter, to source, acting as base, forms a diode of the P-GCMOSFET that gets forward biased such that a first part of Electrostatic discharge event current is shunted to ground via the P-epi and substrate layers; a second part of the electrostatic discharge event current is shunted through the parasitic PNP transistor of the GC-MOSFET to ground via the electrostatic discharge protection device on the VCC pad as its parasitic NPN transistor is turned ON; a third

part of the Electrostatic discharge event current flows through N-GC-MOSFET, and a parasitic NPN transistor of GC-MOSFET turns on during an electrostatic discharge event and the third part of the electrostatic discharge current is shunted to ground.

11. A N-channel MOSFET structure for electrostatic discharge device, the structure comprising:

a P-doped substrate having an epitaxial layer for forming active device elements therein; and

within said epitaxial layer,

a N+ doped source region,

a N+ drain region,

a P-doped channel region between the source region and the drain region,

a gate superjacent the channel,

an N-doped well region beneath said drain region having a width dimension less than a width dimension of said drain region, and

a P-doped deep region, beneath said drain region and adjacent said well region, having a dopant concentration greater than said P-doped channel region,

wherein said P-doped deep region increases gain of a parasitic lateral NPN transistor formed by said source region, said channel region and said drain region and lowers triggering voltage of said MOSFET.

12. A P-channel MOSFET structure for an electrostatic discharge protection circuit,

the structure comprising:

a P-doped substrate having an epitaxial layer;

an N-doped well in said epitaxial layer for forming active device elements therein; and

within said N-doped well,

a P+ doped source region,

a P+ drain region,

a N-doped channel region between the source region and the drain region,

a gate superjacent the channel, and

a P-doped deep region, beneath said drain region and adjacent said well region,

wherein said P-doped deep region increases gain of a parasitic PNP transistor formed by said drain region, N-doped well region and said epitaxial layer and lowers triggering voltage of said MOSFET.

13. A MOSFET structure for an electrostatic discharge protection circuit, the structure comprising:

a substrate having an epitaxial layer forming an active device surface;

at least two MOSFETs proximate said surface, each MOSFET having a first dopant type drain region wherein said drain regions are adjacent and separated by a region of said surface and forming diode poles thereby; and

a second dopant type deep region at said region of the surface, wherein said

deep region has a depth from said surface into said epitaxial layer greater than a depth of each of said drain regions such that an electrostatic discharge spike causes a diode breakdown to the epitaxial layer before affecting the MOSFETs.

14. The structure as set forth in claim 13 wherein said deep region has a predetermined P-type ion concentration and predetermined dimensions such that an electrostatic discharge spike at said drain will cause a diode breakdown through epitaxial layer and substrate before affecting the MOSFETs.

15. A MOSFET structure for an electrostatic discharge protection circuit employing an SCR, the structure located in an epitaxial layer of a first dopant type of a substrate, said epitaxial layer having an active device surface, the structure comprising:

a first MOSFET of a second dopant type located proximate said surface and having a first drain region of the second dopant type;

a second MOSFET of the second dopant type and located proximate said surface and having a second drain region of the second dopant type proximate said first drain region;

a drain contact electrically connecting said first drain region and said second drain region;

a surface contact region abutting said drain contact and separating said first drain region said second drain region, said surface region having said first dopant type;

subjacent the surface contact region and within said epitaxial layer, a well of said second dopant type, wherein said well is subjacent both said first drain region and said

second drain region; and

within said well, a deep region of P-type ion dopant, wherein said deep region is subjacent both said first drain region, said second drain region, and said surface contact region,

wherein said deep region dimensions and concentration of the P-type ion are predetermined for achieving a desired SCR punch-through voltage via tuning breakdown fields and improving structure inherent bipolar transistor gain accordingly.

16. The structure as set forth in claim 15 wherein punch-through voltage of the SCR is controlled by the spacing between the deep region and P-wells.

17. The structure as set forth in claim 15 wherein during a positive electrostatic discharge spike to an I/O pad associated with the structure, the SCR being in parallel with the N-channel MOSFETs conduct a significant amount of current, enhancing electrostatic discharge protection.

18. A BiCMOS technology N-MOSFET structure for electrostatic discharge protection circuits, the structure comprising:

a P ion doped substrate;

an N ion doped epitaxial layer superjacent said substrate, said epitaxial layer having an upper surface distal from said substrate;

a buried isolation layer;

a P ion doped well subjacent in said upper surface;

a N+ ion doped source region subjacent said surface;

a N+ ion doped drain region subjacent said surface;

a region of said well forming a P ion channel region at said surface between said source region and said drain region;

a gate structure superposing said channel region; and

subjacent said drain region and within said well, a P ion doped deep region, said deep region having an ion concentration greater than ion concentration of said well,

such that lateral bipolar parasitic NPN transistor of said structure is provided with increased gain by the deep region.

19. A BiCMOS technology P-MOSFET structure for electrostatic discharge protection circuits, the structure comprising:

a P ion doped substrate;

an N ion doped epitaxial layer superjacent said substrate, said epitaxial layer having an upper surface distal from said substrate;

a buried isolation layer;

a N ion doped well subjacent in said upper surface;

a P+ ion doped source region subjacent said surface;

a P+ ion doped drain region subjacent said surface;

a region of said well forming a N ion channel region at said surface between said source region and said drain region;

a gate structure superposing said channel region; and

subjacent said drain region and within said well, a P ion doped deep region, said

deep region having an ion concentration substantially equal to or greater than ion concentration of said drain region,

such that vertical bipolar parasitic PNP transistor of said structure is provided with increased gain by the deep region.

20. A BiCMOS technology structure for a push-pull Input-output electrostatic discharge protection circuit employing an SCR, the structure located in an epitaxial layer of a first dopant type of a substrate of a second dopant type, said epitaxial layer having an active device surface, the structure comprising:

a first dopant type buried layer segregating said epitaxial layer and said substrate;

a second dopant type first well within said epitaxial layer and subjacent said surface;

a second dopant type second well within said epitaxial layer and subjacent said surface;

a first dopant type third well within said epitaxial layer and subjacent said surface, such that third well is adjacently between said first well and said second well;

a first MOSFET of the first dopant type located within said first well proximate said surface and having a first drain region of the first dopant type and having a predetermined drain width for superjacently spanning a first area of said surface encompassing surface regions of both said first well and said third well;

a second MOSFET of the first dopant type and located within said second well proximate said surface and having a second drain region of the first dopant type and

having a predetermined drain width for superjacently spanning a second area of said surface encompassing surface regions of both said third well and said second well;

a drain contact electrically connecting said first drain region and said second drain region;

a surface contact region abutting said drain contact and separating said first drain region said second drain region, said surface region having said second dopant type;

within said third well, a deep region of P-type ion dopant, wherein said deep region is subjacent both said first drain region, said second drain region, and said surface contact region,

wherein said deep region dimensions and concentration of the P-type ion are predetermined for achieving a desired SCR punch-through voltage via tuning breakdown fields and improving structure inherent bipolar transistor gain accordingly.

21. An extended drain N-channel MOSFET structure comprising:

a P-type substrate;

in said substrate at least one MOSFET structure having extended and enhanced drain region devices for providing reduced on-resistance at a surface region of said substrate, said MOSFET structure including an N+ doped drain region in an N-type well region; and

a P-deep region subjacent the N-well containing the drain region, said P-deep region having geometry and a dopant concentration such that said P-deep region increases gain of a parasitic lateral NPN transistor and lowers triggering voltage of said MOSFET, improving electrostatic discharge tolerance thereby.